FPGA Based Five-Phase Sinusoidal PWM Generator

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Abstract—**Multiphase machine has became popular in many rotational drive applications due to its reliability, high efficiency and high quality of waveforms. Moreover, this machine (e.g. 5-phase induction machine) can provide more options for selecting the most optimum voltage vector since the number of switching devices of the inverter increases that can enhance torque capability and improve dynamic performances. However, the great advantageous offered cannot be realized if the switching and control strategy performed at very low sampling frequency which does not guarantee for the multiphase drive to operate at optimum operations. This paper presents the realization of five-phase sinusoidal PWM signal generator at fast sampling frequency using one-chip programmable gate array (FPGA). It can be shown that the generation of sinusoidal PWM using FPGA can perform the switching frequency of the inverter at 40 kHz switching frequency that may raise potential for excellent drive performances.**

Keywords-Five-Phase Sinusoidal PWM Generator, FPGA, inverter, motor drives, power converter, VHDL

I. INTRODUCTION

In recent years, attention in multiphase inverter technology has increased due to the benefits of using more than three phases in drive applications. Multiphase motor possess several advantages, such as reduced the amplitude and increased the frequency of torque pulsations, reduced rotor harmonics currents, reduced dc-link current ripple, reduced stator current per phase without increasing the voltage per phase, increased fault tolerance, greater efficiency, lower per phase power handling requirements, improved noise characteristics, and higher reliability as compared to a three-phase motor [1-6]. In general, the 5-phase machines produce the output current 6-8% higher than those of the 3-phase and 6-phase machines [7]. The most commonly used of multiphase system which is the smallest phase number, is five-phase.

Several work on design and control of five-phase ac motor drives were published, and also a lot of modulation techniques for five-phase pulse width modulation (PWM) inverters have developed [8-12]. However, different from three-phase PWM inverters, till recently, not much works had been made in FPGA-based multiphase PWM signal generating that results in minimal input and output ripple on five-phase PWM inverters. In [13], a early model of sinusoidal PWM waveform generation for a five-phase converter using FPGA technology is presented. No work has considered as to what is the optimum technique that result has been investigated and in minimum current ripples. In this paper, five-phase carrier-based sinusoidal PWM signal generator utilizing FPGA is presented. Relationship of the voltage vectors and switching states between three-phase and five-phase system will be reviewed in section II, and the relevant expressions are derived. Section III describes principle of five-phase PWM generating, that its implementation is showed in section IV. Results and discussions are presented in section V, and in section VI conclusion is drawn.

II. GENERAL EXPRESSIONS

Figure 1 shows the number of switching states (or voltage vectors) provided by the 3-phase induction machine-drive system.

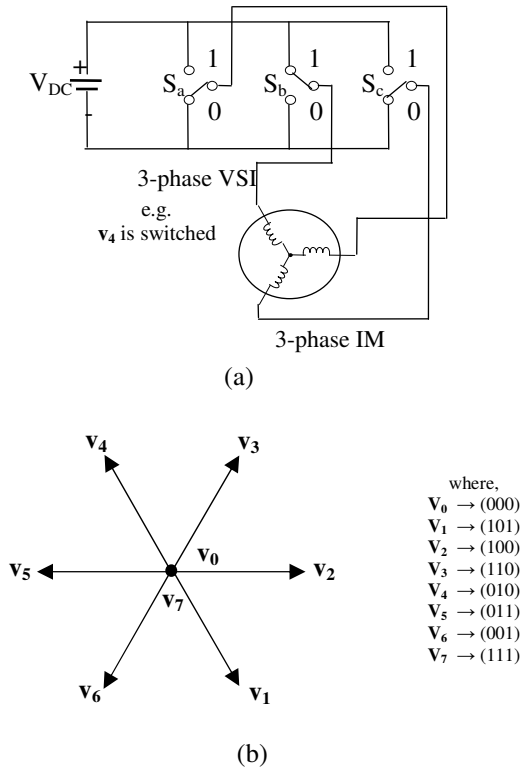
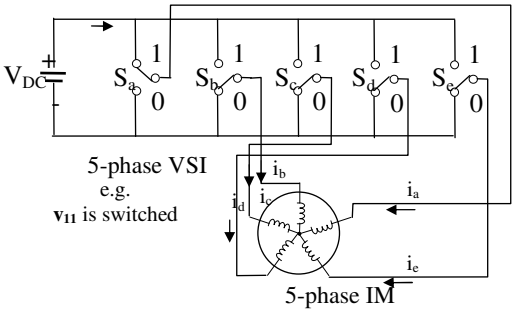


Figure 1. Voltage vectors and switching states in 3-phase induction machine-drive system; (a) power circuit configuration and (b) space voltage vectors plane

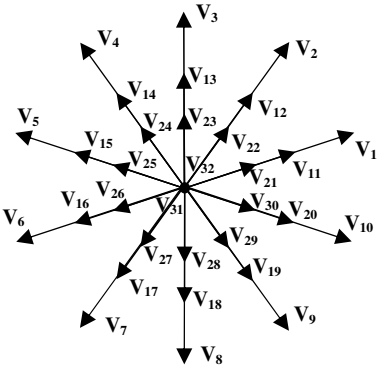
The 3-phase motor drives are supplied with a 3-phase voltage source inverter (VSI) which can only have 2^3= 8 voltage vectors. Figure 2 shows the number of switching states (or voltage vectors) provided by 5-phase induction machine-drive system. In comparison with 3-phase induction motor drives, the 5-phase motor drives are supplied with a 5-phase voltage source inverter (VSI) which can have 2^5=32 voltage vectors (i.e. 2^n where n is the number of phase). In particular, the 32 space voltage vectors are composed of three sets of vectors having different amplitudes and divide the voltage vector plane into ten sectors. The relationship among the DC side current, switching states and the AC side current of the inverter with refer to Figure 2.a can be written as

$$i_d = s_a i_a + s_b i_b + s_c i_c + s_d i_d + s_e i_e \qquad (1)$$

where s_a, s_b, s_c, s_d and s_e are the switching states of phase 1, 2, 3, 4 and 5, respectively.



(a)



where,

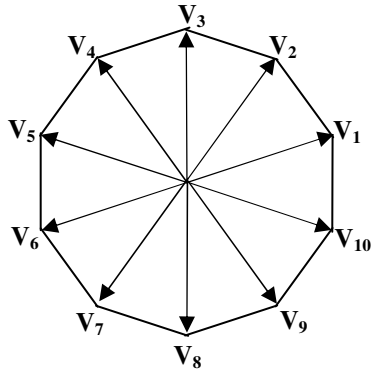
$V_1 \rightarrow (11001)$	$V_2 \rightarrow (11000)$
$V_3 \rightarrow (11100)$	$V_4 \rightarrow (01100)$
$V_5 \rightarrow (01110)$	$V_6 \rightarrow (00110)$
$V_7 \rightarrow (00111)$	$V_8 \rightarrow (00011)$
$V_9 \rightarrow (10011)$	$V_{10} \rightarrow (10001)$
$V_{11} \rightarrow (10000)$	$V_{12} \rightarrow (11101)$
$V_{13} \rightarrow (01000)$	$V_{14} \rightarrow (11110)$
$V_{15} \rightarrow (00100)$	$V_{16} \rightarrow (01111)$
$V_{17} \rightarrow (00010)$	$V_{18} \rightarrow (10111)$
$V_{19} \rightarrow (00001)$	$V_{20} \rightarrow (11011)$
$V_{21} \rightarrow (01001)$	$V_{22} \rightarrow (11010)$
$V_{23} \rightarrow (10100)$	$V_{24} \rightarrow (01101)$
$V_{25} \rightarrow (01010)$	$V_{26} \rightarrow (10110)$
$V_{27} \rightarrow (00101)$	$V_{28} \rightarrow (01011)$
$V_{29} \rightarrow (10010)$	$V_{30} \rightarrow (10101)$
$V_{31} \rightarrow (11111)$	$V_{32} \rightarrow (00000)$

(b)

Figure 2. Voltage vectors and switching states in 5-phase induction machine-drive system, (a) power circuit configuration and (b) space voltage vectors plane

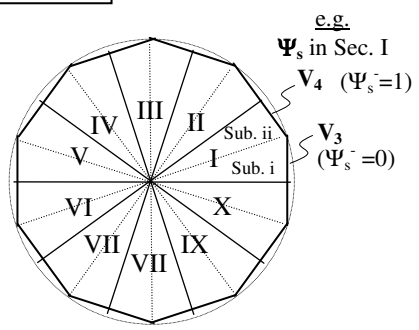
Figure 3 illustrates the stator voltages, i.e. 10-step voltage that can be established in 5-phase inverter by controlling the flux vector trajectory into decagonal shape, as Figure 3(a). If it is required, the formation of decagonal flux locus can be accomplished by modifying the flux error status according to flux positions. For clearer picture, the trajectory of flux in Sector I to form a decagonal flux shape with modified flux error status is shown in Fig. 3(b). In this sector, the modified flux error status Ψ_s^- is equal to 0 to increase the flux ($\mathbf{V_3}$ is selected) whenever the flux lies in subsector i, otherwise the Ψ_s^- is equal to 1 to decrease the flux ($\mathbf{V_4}$ is switched) whenever the flux lies in subsector ii.

(a)



$\Delta\Psi_s = V_{s,k} \cdot \Delta t$

(b)



(c)

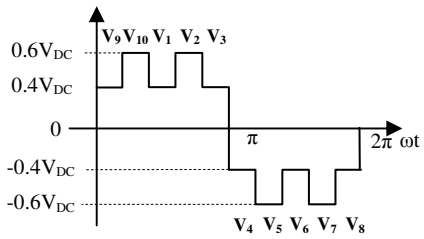


Figure 3. Decagonal flux locus with application of 10-step Voltage; (a) voltage vector plane, (b) stator flux plane, (c) phase voltage

In general, if the sector k is equally subdivided into Subsectors, i and ii, voltage vector of two possible voltages that uses to increase the flux (Ψ_s^- is equal to 0) will be selected throughout Subsector i and voltage vector that uses to decrease the flux (Ψ_s^- is equal to 1) will be used throughout Subsector ii. As the flux vector moves from one sector to another sector until it completely forms a decagonal flux shape, it is possible that the

stator voltage to reach at 10-step voltage limit. This particularly can be achieved when the motor speed exceeds its base speed where the application of zero voltage vectors is zero. It should be noted that the torque demand will be naturally fulfilled by the controller, which will gradually drops the applications of zero voltage vectors as the speed increases approaching its base speed. As the speed is further increased and no more zero voltage vectors are available, the selection of voltage vector will naturally transform to 10-step mode. In other words by transforming the stator flux locus to the decagonal shape, we provide the room for the stator voltage to increase beyond the decagonal boundary and the torque demand will naturally transform the stator voltage from PWM to 10-step mode.

The on-off signals for the switching devices can be obtained by comparing five-phase reference signals or modulated signals to a high-frequency triangular signal as carrier signal. Figure 4 shows the phase reference signals used in this paper, which can be written as

$$\begin{aligned} V_{ref1} &= k \sin\theta + v_{inj} \\ V_{ref2} &= k \sin(\theta - \frac{2\pi}{5}) + v_{inj} \\ V_{ref3} &= k \sin(\theta - \frac{4\pi}{5}) + v_{inj} \\ V_{ref4} &= k \sin(\theta - \frac{6\pi}{5}) + v_{inj} \\ V_{ref5} &= k \sin(\theta - \frac{8\pi}{5}) + v_{inj} \end{aligned} \quad (2)$$

where v_{inj} is an arbitrary signal that is injected into the sinusoidal reference signals. Because the injection signal into the phase reference signals is same, the average value of the phase-to-phase voltages will not be altered by this arbitrary signal. The arbitrary signal assumption is valid as long as the frequency of carrier (triangular) signal is much higher than the reference signals. In this condition, the reference signals can be assumed as constants during one carrier period, and the detailed inverter waveforms can be drawn as shown in Figure 5. The figure is valid during the interval A of Figure 4.

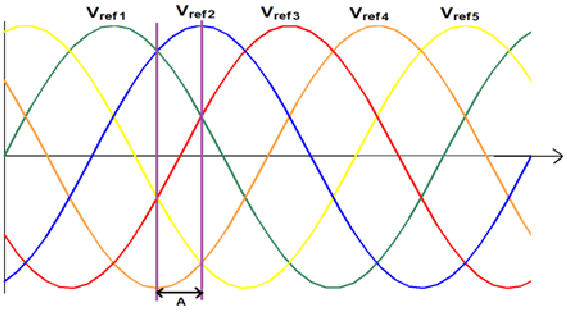


Figure 4. Five reference signal

By using eq.(1), the dc input current during one carrier period, as shown Figure 5, can be written as

$$i_d = \begin{cases} 0, & \text{for } t_0 \le t \le t_1 \\ i_b, & \text{for } t_1 \le t \le t_2 \\ i_a + i_b, & \text{for } t_2 \le t \le t_3 \\ -i_d - i_e, & \text{for } t_3 \le t \le t_4 \\ -i_d, & \text{for } t_4 \le t \le t_5 \\ 0, & \text{for } t_5 \le t \le t_7 \\ -i_d, & \text{for } t_7 \le t \le t_8 \\ -i_d - i_e, & \text{for } t_8 \le t \le t_9 \\ i_a + i_b, & \text{for } t_9 \le t \le t_{10} \\ i_b, & \text{for } t_{10} \le t \le t_{11} \\ 0, & \text{for } t_{11} \le t \le t_{12} \end{cases} \quad (3)$$

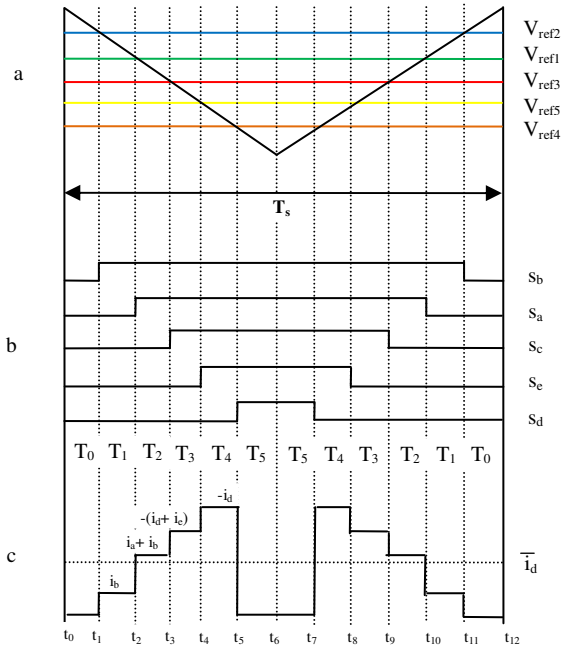


Figure 5. Inverter waveforms over one carrier period

III. FIVE-PHASE SPWM ALGORITHM IMPLEMENTATION

Figure 6 shows the design of overall experimental set-up. However, the paper only focus on FPGA based five-phase sinusoidal PWM signals generating, and the overall system is under preparation.

Due to limitation the allocated space, in depth design procedure of PWM signal generator that is easy for modifying cannot be presented. However, the overall system is hoped provide clear enough about this research in future and have capability to involve many researches in next development phase.

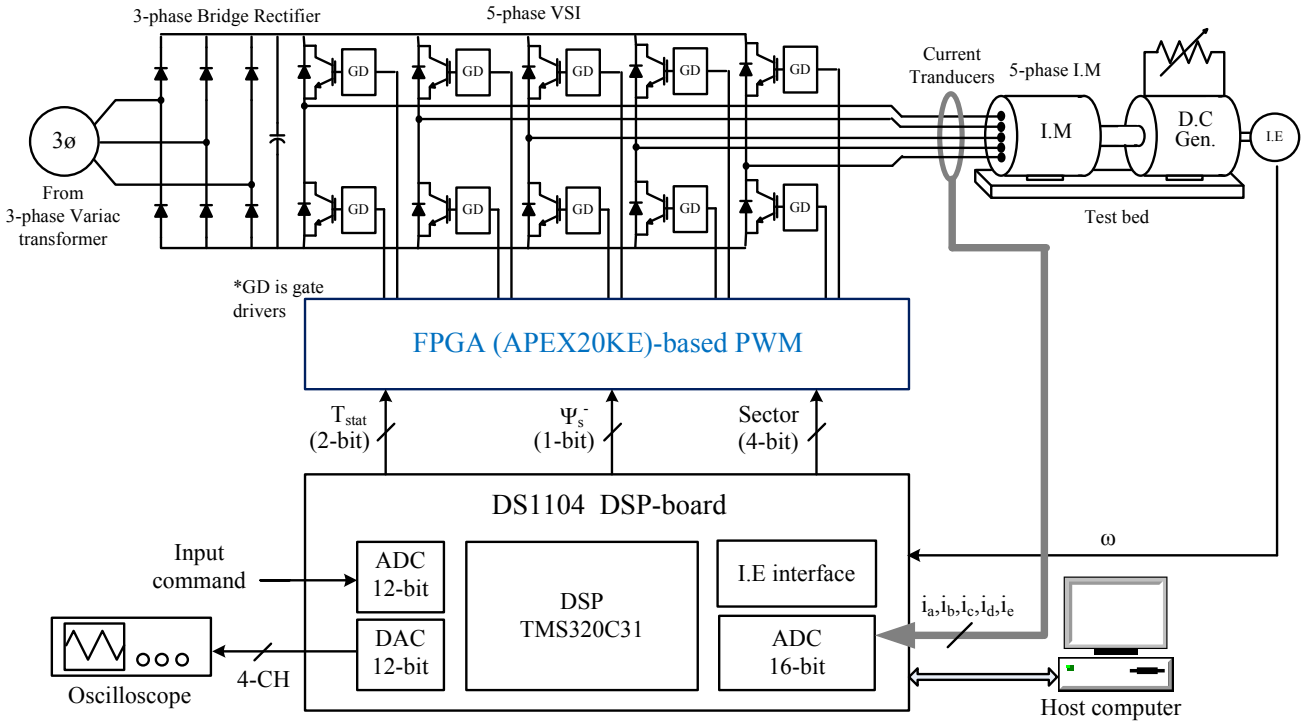
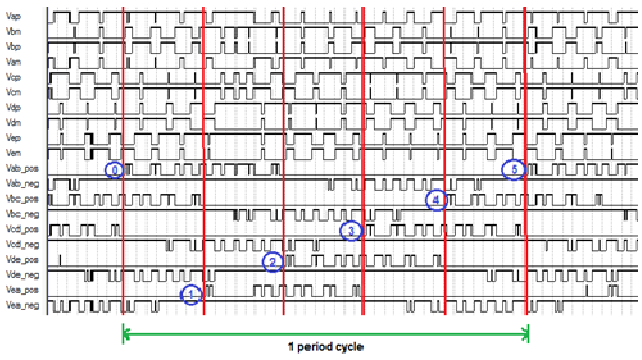
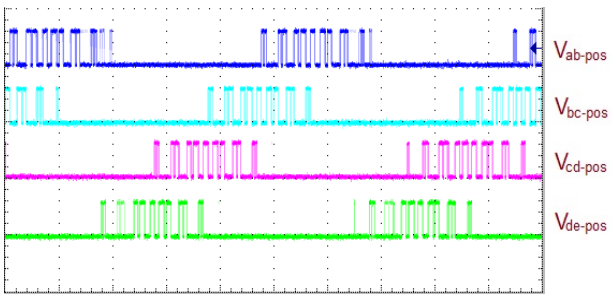


Figure 6. Design of overall experimental set-up

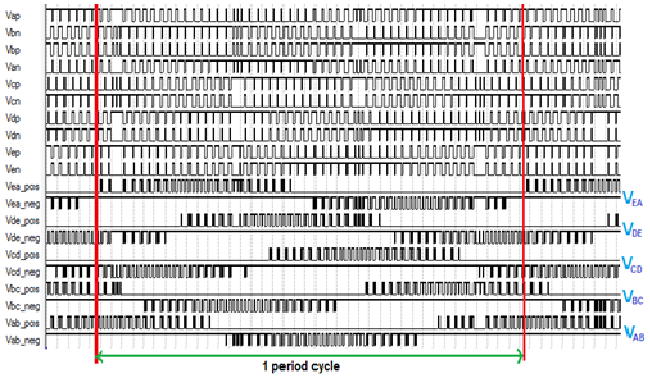


a



b

Figure 7. PWM signal generator in lower switching frequency, (a) Quartus result simulation, (b). FPGA implementation result



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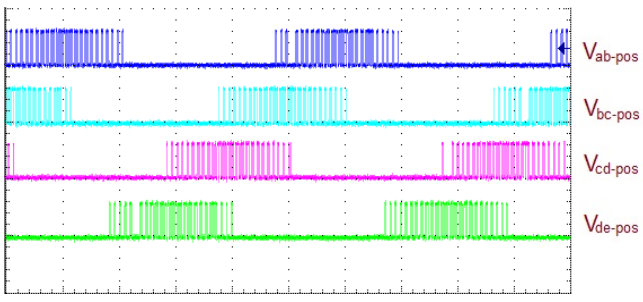

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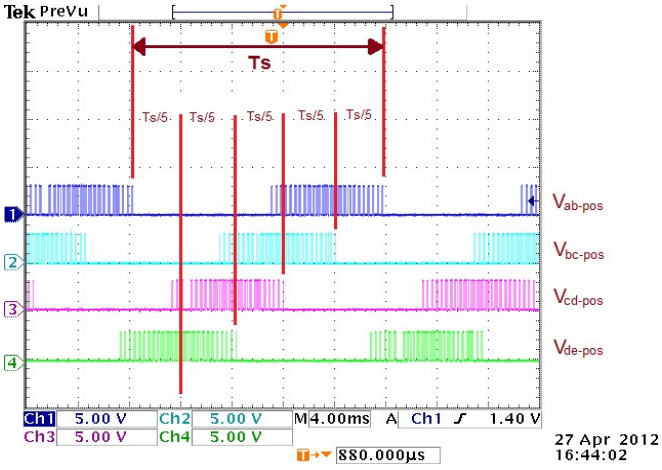
Figure 8. PWM signal generator in higher switching frequency, (a) Quartus result simulation, (b). FPGA implementation result

IV. Results and Discusions

The five-phase sinusoidal PWM modules are described with mix VHDL and schematic entry design using Quartus II software. After placement and routing, the design is implemented in Altera APEX20KE, where 496 logic elements are used. The designed IC can operate at 33MHz system clock, and the switching frequency is adjustable. Figure 7 shows simulation and implementation result of PWM signal generator in switching frequency lower than Figure 8. From Figure 7 (a) is clear that the PWM signals shift $2\pi/5$ rad. The phase shifting in hardware implementation is shown in Figure 9 (a). In Figure 9(b), leg pair of PWM signals on switching frequency higher than Figure 7(b) and 8 (b) is presented. Therefore, the PWM signals are ready to implement for controlling five-phase inverter s.



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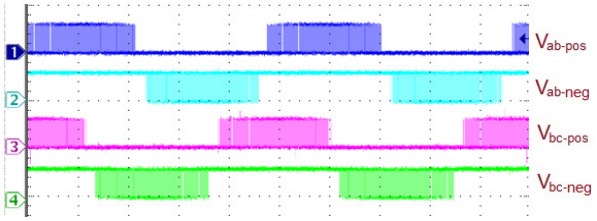

b

Figure 9. PWM signal generator based on FPGA,
(a) Phase shifting of PWM signals, (b). Leg pair of PWM signals on highest switching

V. Conclusion

This paper presents the realization of a programmable five-phase sinusoidal PWM signal generator based on FPGA. Relationship of the voltage vectors and switching states between three-phase and five-phase system have been reviewed, and the relevant expressions have been derived, and then principle of five-phase PWM generating have been described. The proposed scheme was implemented and tested using an FPGA technology. Experiment results show that the constructed design can acquire excellent operating performance. It is believed that such five-phase PWM control IC's will become key components in power converter and motor drives of the future.

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