High efficiency Doherty Power Amplifiers for modern wireless communication systems: a brief review

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ABSTRACT

Due to the high peak to average power ratio (PAPR) of modern modulated signals, Power Amplifiers (PAs) have been forced to operate at the back-off (BO) region of their saturation power in order to avoid signal clipping and distortion. However, classical PAs such as class AB suffer from low efficiency when they operate in the BO region. Therefore, efficiency has to be enhanced in this region. To do so, many techniques have been proposed. Among them, the Doherty power amplifier (DPA) is considered as the most suitable technique due to its simple structure and high performance. However, its conventional design is limited to a 6 dB BO level which does not satisfy the requirements of modern communication systems. In this paper, a brief review of the most significant techniques of high-efficiency DPA is presented. First, DPA topology and its operation principles are briefly discussed. Second, efficiency enhancement techniques such as an asymmetrical DPA, output combiner modification, gate bias adaption, offset line optimization, and multi-way DPA were discussed. The study shows that the most suitable, simple, and effective solution is an asymmetrical approach. However, it needs to be investigated in terms of bandwidth in order to meet the efficiency-bandwidth requirements of modern wireless communication systems such as 5G.

Keywords:

Doherty Power Amplifier
High Efficiency
Back-off
Wireless Communications
5G

1.   INTRODUCTION

Modern wireless communication systems use complex modulation schemes such as Orthogonal Frequency Division Multiplexing (OFDM) with high order Quadrature Amplitude Modulation (QAM) to make better use of the available limited frequency spectrum in order to produce high data rates. However, those modulated signals are characterized by a high peak-to-average power ratio (PAPR), meaning that the waveform in the time domain presents rare peaks significantly higher than the average ones, as shown in figure 1. In order to amplify modulated signals with a high PAPR, the PA's output power has to be backed-off from saturation by the same amount of PAPR. However, conventional PAs such as class AB suffer from low efficiency at the back-off (BO) region as their efficiency is determine at the maximum output power. To solve this problem, efficiency has to be enhanced at the BO region. To do so, several techniques have been proposed, such as the outphasing power amplifier [2], Doherty amplifier [3], and sequential power amplifier [4]. Among the above-mentioned techniques, the Doherty Power Amplifier (DPA) is considered as the most suitable technique due to its simple structure, ease of implementation, and high performance [5-9]. However, conventional DPAs can only maintain moderate efficiency at 6 dB BO level [10], which does not satisfy the requirements of modern wireless communication systems.

Figure 1. High Peak-to-Average Power Ratio signal in the time Domain [1]

In this paper, we provide a brief overview of the most important BO's efficiency enhancement techniques proposed for improving the efficiency of conventional DPAs. The rest of the paper is organized as follows: Section 2 provides a brief overview of the DPA topology and its operating principles. Section 3 explores the most significant efficiency enhancement techniques. Finally, a conclusion is drawn in section 4.

2. DOHERTY POWER AMPLIFIER

The Doherty amplifier was invented by William H. Doherty in 1936, [3]. It consists of two amplifiers called the main (carrier) amplifier and the auxiliary (peaking) amplifier connected in parallel and biased in class-AB and Class-C respectively, as shown in figure 2. Both amplifiers are connected through a quarter-wavelength impedance inverter which acts as a load modulation network. The phase difference generated by the impedance inverter is compensated at the input of the peaking stage using a delay line. Offset lines are used at the output of the main and auxiliary amplifiers. The main DPA's offset line is used to enhance its efficiency at the BO (i.e. when the peaking is off) while the auxiliary 's offset line is used to prevent power leakage from the main path during the off-state. A power divider is used at the input to divide the power to both amplifiers. Matching network is used at the output of the DPA to match the impedance at the combining point to the 50-ohm system impedance. The working principle of DPA is as follows: In the low power region, only the main stage is working while the peaking is off. Until a certain power level (break point), when the main amplifier reaches its saturation state, the auxiliary turns on and starts to conduct the current. In this way, the BO's efficiency could be enhanced.
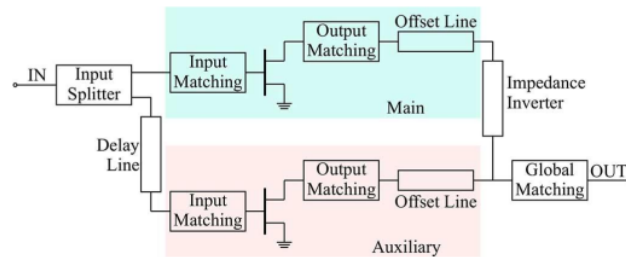
Figure 2. Block diagram of standard DPA [3]

3. EFFICIENCY ENHANCEMENT TECHNIQUES

Standard DPAs have shown a good efficiency performance at 6 dB BO level. However, modern wireless communication systems ask for BO levels in the range of 8-12 dB BO. Therefore, different approaches have been proposed in the literature to enhance the efficiency at a large BO. In this section, we will critically review a variety of innovative designs, describing their advantages and limitations.

3.1. Asymmetrical DPA

To compensate for the low current delivered by the peaking stage, an asymmetrical DPA has been proposed [11-15]. In [11], the asymmetrical operation is achieved by using two times larger transistor for the peaking stage to overcome low power and imperfect load modulation. Although this work has better linearity and good efficiency, around 5 % higher than the conventional DPA [3]. However, using very large transistors leads to increasing the production cost. Furthermore, the low the current peaking stage issue cannot be completely resolve [12]. To solve this problem, an uneven power divider approach has been proposed [12]. In this method, the power divider is designed to deliver power to the auxiliary branch more than that delivered to the main branch to compensate for its low current. In this way, the same current from both amplifiers can be delivered and proper load modulation can be achieved. As a result, proper load modulation can be achieved, leading to the BO's enhancement. In spite of that, the low power delivered to the main amplifier has resulted in a low gain. As a result, because the full DPA's gain is primarily dependent on the gain of the main amplifier. Therefore, the full DPA's gain and output power are reduced. Another method of achieving asymmetrical DPA is to feed the peaking stage with a high drain bias voltage greater than that of the carrier amplifier, as in [13], [14], and [15]. According to the study in [12], by lowering the carrier amplifier's drain voltage, the BO's efficiency is increased by 3.43% when compared to the conventional DPA. However, the maximum output

power is reduced. This is due to the low bias voltage of the carrier amplifier, which leads to a low gain and output power. As a result, the overall DPA's gain and output power is reduced.

3.2. Output Combiner Modification

Another good investigation in the literature has been given to the modification and optimization of the output combiner of the conventional DPA. In the work of [16], characteristic impedances of load modulation network (impedance inverter and global matching) are adjusted to solve the problem of incomplete load modulation caused by current unbalance between carrier and peaking amplifiers. Measurements results show an efficiency enhancement of 8% and 13 % at saturation and BO respectively, when compared with the conventional DPA. In [17], the characteristic impedance of the output matching network is modified based on the current and power ratios between the carrier and the peaking amplifier in order to achieve correct load modulation and enhance the efficiency. A prototype was developed at 3.45 GHz using symmetrical devices and even power divider. The efficiency is improved by 2-3 % with respect to the conventional DPA. A different approach is proposed in [18], where the load modulation network of the conventional DPA is replaced with two quarter-wavelength impedance transformers and a shunted reactive load for efficiency-bandwidth enhancement simultaneously, as shown in figure 3. The proposed circuit is fabricated and measured for validation purposes. Although the measured results showed an improvement in efficiency at the BO level. However, it is still limited to 6 dB BO.
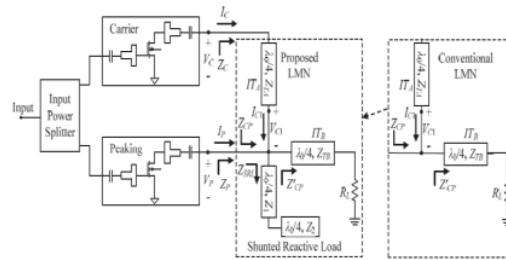

Figure 3. Block diagram of the DPA presented in [18]

3.3. Multi-way DPA

The Multi-way DPA consists of a number (N) of identical devices (N > 2), one for the carrier stage and N-1 for the peaking stage, as shown in figure 4 [12]. Unlike the conventional two-way DPA, which has two peak efficiencies, one at the BO and the other at the peak output power. Additional peaks at different BO levels can be produced by a multi-way DPA based on the number of the peaking devices. For example, the 3-way DPA can introduce three peaks, two at different BO points and one at the peak. By introducing additional BO levels, the efficiency of the BO will be extended. The work of [19] implements a 3-way DPA using three 30 watt devices, one for the carrier and two for two separate peaking amplifiers. The measured results show drain efficiency of 28-33 % at 8-10 dB BO. Another 3-way DPA is presented in [20] with a high BO level of 12 dB. However, it requires a complex mixed signal setup to control the input power of the amplifiers. The work of [21] proposed a 3-way DPA with a high BO level of 11.7 dB without the need for a complicated mixed-signal setup. Unlike the conventional asymmetrical three-way DPA where three identical devices are used, the work of [22] proposed a symmetrical approach where one 60 W transistor is used for the carrier amplifier and two 30 watts are used for the peaking amplifiers. The proposed design achieves an efficiency of 33.7 % at 6.5 dB BO. Although the achieved BO is low when compared to the conventional three-way DPA. However, it is considered a cost-effective design and is suitable for modulated signals that apply PAPR's reduction techniques. Multi-way DPAs have shown a significant improvement in efficiency at high BO levels. However, it contributes to increasing the circuit size and production cost as multi-devices (transistors) are required.
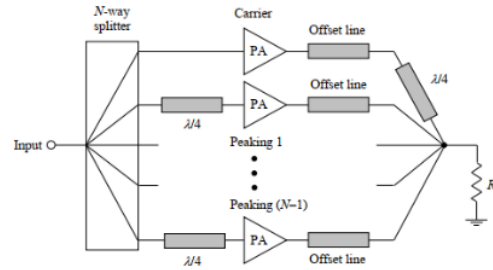
Figure 4. Block diagram of multi-way DPA [23]

3.4. Other Techniques

Other techniques are proposed in the literature, such as switched-mode DPAs. In the work of [24], the conventional Class AB-C DPA is replaced with the Class-F, as shown in figure 5. The measured results show a high efficiency of 50 % is achieved at 7 dB BO, which is 8% higher with respect to the conventional DPA. However, the Class-F PAs suffer from nonlinearity issues due to operating in saturation mode [25]. Therefore, digital pre-distortion (DPD) combined with PAPR reduction techniques are applied to meet the linearity requirements. In other work [26], a blended class-EF mode is proposed. Load-pull analysis is used to determine the load impedance at the fundamental frequency. Whereas, load impedance at harmonic frequency is set according to class-EF requirements. The proposed design achieves high efficiency at both peak output power and at the BO region. The measured results show efficiency of 81.3% and 68% at both the peak and BO regions, respectively. The Gate bias adaptation technique was proposed in [10] to solve the problem of BO's efficiency degradation of the conventional DPA. In this technique, the gate biases of both amplifiers are adaptively adjusted as the input power increases by using an external control circuit to achieve proper load modulation [12]. The work of [10] proposed DPA implemented gate bias adaption technique. The gate bias of the carrier is controlled so that the peak power with the optimum load is increased. The measured results show high efficiency, over 62% at 6 dB BO. The work of [27] optimized the carrier's offset line to compensate for phase mismatch at the BO associated with conventional DPA. The characteristic impedances of the carrier's offset line and impedance inverter are set to $R_0/2$, which is the same load impedance at the BO, instead of R_0 in conventional DPAs. In this way, the design sensitivity is moved from the BO region, which is more important for modulated signals with high PAPR, to the peak region. The proposed design achieves a high efficiency of 60.7% at 6.5 dB BO, while showing a degradation of peak output power of less than 0.01 dBm. Significant progress in BO extension is shown in [28], where a large BO level of 15 dB is achieved. By controlling the input power of the carrier DPA, the variation range of its optimum output impedance can be reduced and the efficiency over a large OBO could be enhanced. For verification, the prototype was developed at 2.56 GHz using GaN-HEMT devices. Measurement results show a DE of 58-63% at 15 dB OBO with an average output power of 28 dBm. Although a large BO level is achieved in this work. On the other hand, the proposed design needed to be tested to verify its linearity performance. In contrast to conventional DPAs, load modulation is achieved in [29], [30] without the use of a quarter-wavelength impedance inverter. In this design, the impedance seen by the main amplifier is modulated according to the current contributed by the peaking amplifier. The proposed design achieves an efficiency of 50% at 6 dB BO and it can contribute to reducing the occupied area.
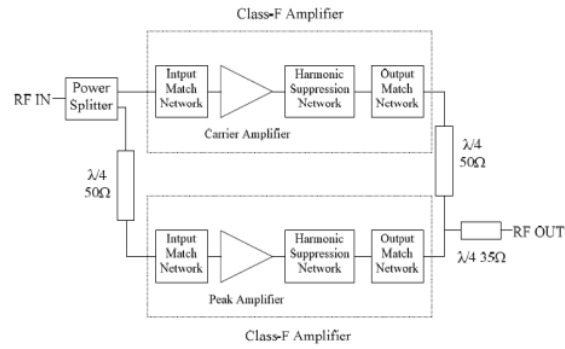
Figure 5. Class-F Doherty power amplifier [24]

4. CONCLUSION

In conclusion, the most recent literature on efficiency enhancement techniques of the Doherty power amplifier has been reviewed and critically discussed. The main drawback of each technique has been highlighted. Different techniques have been discussed, such as an asymmetrical DPA, output combiner modification, multiway DPA, continuous-mode DPAs, gate bias adaption, and offset line optimization. Among the proposed techniques, asymmetrical approach can be considered as a simple and straightforward solution to enhance the BO's efficiency. However, it has a limited bandwidth. As a result, bandwidth extension technique can be used in conjunction with it to evaluate the efficiency over a wide-bandwidth.

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