Passive damper network in a simple DC distribution power system

By Jusoh A.B

Passive Damper Network in a Simple DC Distribution Power System

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ABSTRACT

Distributed power system (DPS) distributes power amongst processing units such as power electronics converters with DC system. Due to the increasing usage of power converters in DPS system, the system becomes unstable and the converter tends to draw constant power needed by the load of the system. Constant power load (CPL) characteristic has negative input impedance that could produce instability problems in the DC bus system. Passive damping network which consists of series RC damping circuit was connected in parallel to the DC bus system with the purpose to reduce the instability. The passive damper was designed, simulated with MATLAB/Simulink and verified experimentally with different values of CPL power levels and input voltage changes. The obtained simulation results show that simple DC system with constant power load was successfully stabilized by the installation of the passive damping network. The experimental set up was also conducted to validate of the proposed technique, and the obtained results were in excellent agreement with the theoretical parts of the project.

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1. INTRODUCTION

Distributed power system (DPS) uses direct current (DC) bus bar to distribute power among processing units such as power electronics converter or DC/DC converters [1], [2]. DPS mostly applied in major industry around the world such as in aircraft, industrial systems, communication systems and many more [3]. DPS is a mature technology as an alternative method to deliver power to the end user [4].The advantages are due to its weight, voltage regulation, size and the flexibility of the system [3], [5]. In DPS, the main supply will be connected to the source voltage that used to modulate the output voltage instead of being supplied directly to the load. The output voltages are desirable to be used and meet the load requirement after the regulatory process was done. However, DPS has some disadvantages, especially in stability issues, where the interactions between converters make the system become unstable. Apart from that, it also causes uneven power distribution between parallel connected converters in the system.

1.1. The Causes of Distribution System Instability

There are several weaknesses in the DPS. One of them is the interaction between the individual converters which leads to the instability of the system. The unbalance power distribution amongst parallel converters also led to an unequal distribution of the output current. Consequently, it will cause an outrageous tenseness on some modules and will increase the failure [6]. The instability of the DPS contributed by the interaction between the interconnected sub-systems [7]. There is no guarantee that the stability of one stand-alone system can be maintained when two stable sub-systems are combined together. Even though the system might be well-designed for the stand-alone operation, there is a possibility that there will be an interaction when the sub-system is integrated together [7].

This reaction occurs due to internal control functions of each individual converter, for instance, the regulation of the converter output voltage [6]. Thus, it causes the converter to draw constant power and will have negative incremental input resistance within the bandwidth of the converter control loop [6]. The negative incremental input resistance is the main characteristic of the constant power load. The characteristic demonstrates that the internal controller in the converter will draw more current to meet the constant power demanded by the load if the source voltage shows some decrement [7].

1.2. Constant Power Load (CPL)

The constant power load is a load which consumes fixed amount of power regardless the voltage they received [8]. The primary characteristic of the constant power load is the negative incremental input resistance [3], [9], [10]. This means that it has a hyperbolic characteristic of the voltage against current [6]. CPL can be modeled as a dependent current source, that is i=v/p, where v represents the input voltage and P represents the output power [7]. DC/AC inverter and DC/DC converter are the examples of the CPL. They behaved such that the source converter sees the load as a constant power load [11].

The stability of the bus system will be affected by the converter which acts as constant power load and produces a negative incremental input resistance characteristic [12]. The negative incremental input resistance characteristic leads the internal control function of the converter to draw a constant power required by the load irrespective to any interference in the source voltage [13]. The more the CPL connected, the worse the instability will take place [7]. Figure 1 shows the equivalent circuit of a simple system with a constant power load representing by $-R_L$. The input filter of the CPL is indicated by the LC filter while the main characteristic of the CPL is indicated by $-R_L$. V_0 is the DC bus voltage.

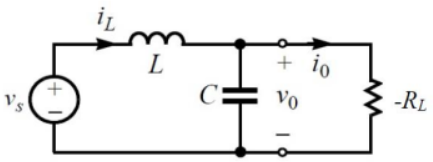


Figure 1. Small-signal schematic diagram of a CPL equivalent circuit

1.3. Negative Incremental Input Resistance Characteristic

Negative load impedance or negative incremental input resistance is the main characteristics associated in power electronic devices such as DC/DC converter. Since each converter has its own internal control function, it draws more current when source voltage falls. This causes the converter to behave such that it attempts to maintain the constant power, which in turn produced negative impedance characteristic [12]. The negative load impedance characteristic of CPL was depicted in figure 2 where it exhibits a hyperbolic shape graph. Based on the graph behavior, it can be seen that as the voltage across CPL increases, the current that flows through it decreases. In contrast, decrease in the output voltage causes increase in the output current.

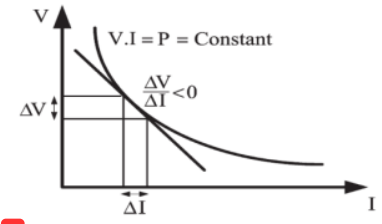


Figure 2. Negative impedance behavior of constant power load

2. PASSIVE DAMPING NETWORK

The implementation of a damper network can help to increase the stability of the DC bus bar voltage. In [8], [14] damper network is divided into two types which are active damping network and passive damping network. The passive damper network is being employed in this paper. Passive damping is generally a network that draws or returns current to the DC bus in order to damp any instability [15]. Passive damping is also widely used to minimize LC filter impedance peaking or dipping [16].

The passive damping network can be achieved by adding resistors in series or in parallel configuration with inductor or capacitor connected to the LC filter [8]. The instability of the arrangement can be minimized by applying either one of the three types of typical passive damping [8].

2.1. Analysis Equations

A simple system comprises of a single source and a single load connected to an interface was analysed in order to comprehend and illustrate the concept of DC bus stability. Figure 3 shows the simple system of impedance based stability standard circuit [7]. The equivalent voltage of the source, impedance of the source, the voltage of the load and the impedance of the load were represented by V_{ts}, Z_s, V_{tL} and Z_L, respectively. The interface bus voltage V is given as Equation (1).

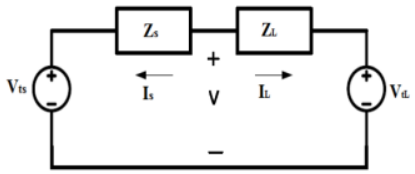


Figure 3. Impedance based stability standard circuit

$$V = \frac{N_L D_S V_{tS} + N_S D_L V_{tL}}{N_L D_S [1 + \frac{N_L D_S}{N_S D_L}]} = \frac{N_L D_S V_{tS} + N_S D_L V_{tL}}{N_L D_S [1 + \frac{Z_S}{Z_L}]} \quad (1)$$

Based on the equation, the numerator and denominator of the source are indicated as NS and DS, respectively while the numerator and denominator of the load are represented by NL and DL [7]. For a load to have a stable operation when it is given with ideal voltage source, an earlier assumption needs to be met. Apart from that, the load also must be a constant current source in order for the source to be operated in stable condition [7]. By referring to the denominator of the equation, the systems are going to be stabled if NL and DS contain no roots in the right half plane. If the magnitude of ZS is always less than the ZL, there will be no encirclement of (-1, 0) point of the Nyquist plot [8].

3. DESIGN OF PASSIVE DAMPING

When capacitor $C_2 \gg C_1$, it is assumed that the value of the impedance of C_2 will be very small at higher frequencies [7]. Therefore, the total resistances that were connected to the output of the filter will be corresponded by the parallel combination of R and R_L, having the value $R_{eff} = \frac{-|R|.|R_L|}{|R|-|R_L|}$ [6]. Based on the observation of this relationship, when $|R_L|<|R|$, the L-C filter will have a net negative damping which causes the filter to oscillate [6].

Thus, to secure system stability, the magnitude of the damping resistor, R, must be lower than the magnitude of the load impedance as discovered by Middlebrook in his impedance stability criterion [17]. Figure 4 shows the equivalent circuit involving LC filter, RC damping network and CPL [18]. RC damper was installed in between the filter network and CPL for the purpose to damp the bus instability which occurs between the input LC filter and CPL.

In order to determine the relationship between the damper and the system stability accurately, the analysis of the system can be shown in Equation (2) and Equation (3) by taking the input-output voltage transfer function into consideration.

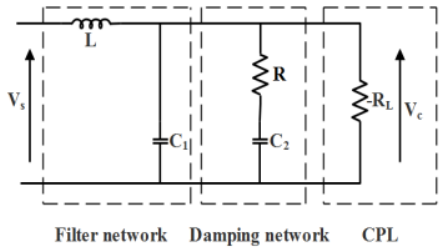


Figure 4. L-C filter with passive damping network and CPL

$$\frac{V_C(s)}{V_S(s)} = \frac{\frac{sRC_2}{LRC_1C_2}}{s^3 + s^2\left(\frac{C_1R_L + C_2R_L - C_2R}{C_1C_2RR_L}\right) + s\left(\frac{C_2RR_L - L}{LC_1C_2RR_L}\right) + \left(\frac{1}{LC_1C_2R}\right)} \tag{2}$$

$$\frac{V_C(s)}{V_S} = \frac{sRR_LC_2 + R_L}{s^3LC_1C_2RR_L + s^2(LR_L(C_1+C_2) - LRC_2) + s(C_2RR_L - L) + R_L} \tag{3}$$

Arranging the denominator in equation in (3), gives Equation (4)

$$-R = -\frac{1}{K} = \frac{s^2(LR_LC_1 + LR_LC_2) - sL + R_L}{s^3LC_1C_2R_L - s^2LC_2 + sC_2R_L} \tag{4}$$

Equation (4) can be factorized as shown in Equation (5)

$$\frac{V_C(s)}{V_S(s)} = \frac{\left[s^2 - \frac{s}{R_L(C_1+C_2)} + \frac{1}{L(C_1+C_2)}\right]\left[\frac{C_1+C_2}{C_1C_2}\right]}{s\left[s^2\frac{s}{C_1R_L} + \frac{1}{C_1L}\right]} = -\frac{1}{K} \tag{5}$$

To get the suitable value for the damping resistor R and capacitor C_2 for maintaining the stability in the system, it can be calculated based on the Equation (6)

$$\left(s + \frac{1}{RC_2}\right)\left(s^2 + s\frac{1}{C_1}\left[\frac{R_L - R}{R_LR}\right] + \frac{1}{LC_1}\right) = 0 \tag{6}$$

Expansion of Equation (6) yields Equation (7)

$$s^3 + s^2\left(\frac{C_1R_L + C_2(R_L - R)}{C_1C_2RR_L}\right) + s\left(\frac{C_2RR_L + \frac{L}{R}[R_L - R]}{LC_1C_2RR_L}\right) + \left(\frac{1}{LC_1C_2R}\right) = 0 \tag{7}$$

By multiplying both Equations in (6) and (7), and by comparing the characteristic between Equation (7) and (3), we noticed that there is an extra term $S\frac{LR_L}{R}$ has appeared. Since the approximate condition for the small-signal stability is $R_L > R$, then for equation (7) to be valid requires $C_2RR_L \gg \frac{LR_L}{R}$ and this resulting in Equation (8)

$$C_2 \gg \frac{L}{R^2} \tag{8}$$

To choose the value for R, C_2 must be chosen first from the Equation (8) in order to ensure the effective resistance in the quadratic portion of Equation (6) provides the satisfactory damping of the complex poles as in Equation (9)

$$R = \frac{R_L\sqrt{LC_1}}{\sqrt{LC_1} + \sqrt{2}C_1R_L} \tag{9}$$

Damping capacitor are obtained from the Equation (10)

$$C_2 = \frac{L}{R^2} \tag{10}$$

4. RESULTS AND DISCUSSION

Figure 5 shows the simulation model for DC system with the insertion of RC parallel passive damping. Based on the calculation theory, the LC filter used are 100 mH and 1000 µF respectively. Furthermore, the passive damping network implemented consists of series R and C_2, which are 6.2 Ω and 3000 µF respectively. These values were selected based on 90 W CPL power level as given in Equation (9) and (10).

Software simulation was used to verify and predict the behavior of the system before proceeding to hardware implementations. The use of circuit simulation on the design can minimize the number of prototypes required and eliminate many repetitive verification procedures. After verification in simulation is performed, implementation on the hardware can be proceeded to verify that the system can be built in real implementation.

The hardware circuit was build as depicted in Figure 6. There are four sectional parts in the designed circuit which are input voltage, LC filter, passive damping network and constant power load. The circuit was designed such that it comes with switches for step input voltage function and to connect passive damper in the DC system. In addition, hole was used for jumper wire connection to measure corresponding voltage and current in the system. The experimental work was conducted using laboratory equipment IT8514C ITECH as DC load bank where the level of CPL power was set accordingly.

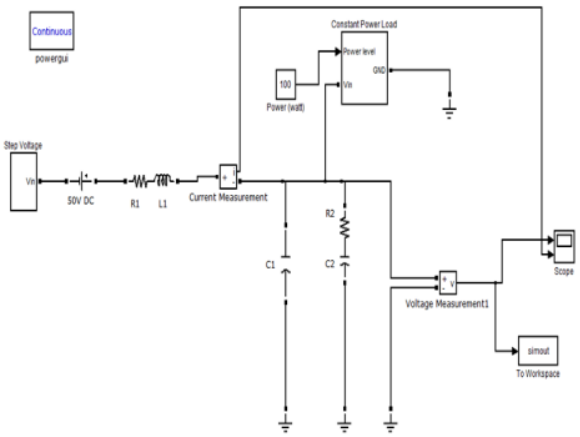


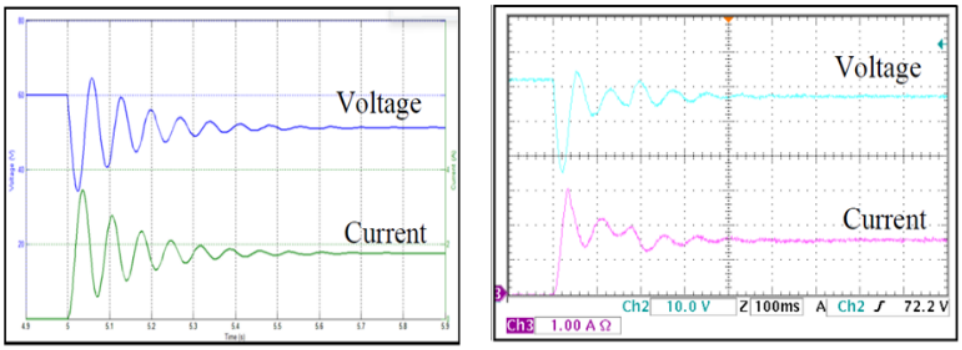
Figure 5. DC system model with RC parallel passive damping

Figure 6. Hardware circuit implementation

4.1. DC Bus Voltages During the Insertion of CPL with Fixed DC Supply without and with Passive Damper

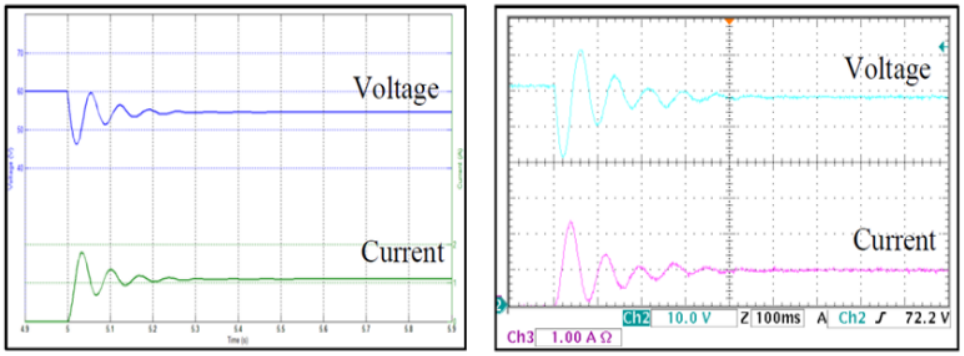
The analysis on system performances with passive damper was carried out based on voltage and current overshoots, settling time and steady state error responses. Table 1 summarizes the comparison between simulation and experiment for overshoots, settling time and steady state error without passive damper connection. The plots in Figure 7, Figure 8 and Figure 9 for three CPL power levels which are 90 W, 60 W and 30 W respectively, shows that when constant power load applied to the system, the voltage and current oscillates and it is settled at to a steady state value. When the constant power load level decreases slightly, the bus voltage oscilaltes and takes a little time to reach its new steady state value. On top of that, when the CPL power level increases, the percentage of overshoot and steady state error has also increased.

For the 90 W CPL power level, the bus voltage between simulation and experiment continue to oscillate for almost 700 ms which is also quite longer when compared with previous 60 W and 30 W CPL level. The difference in the oscillation between these power levels is not much since there is only 30 W CPL level between them but it will increase as the difference increases.



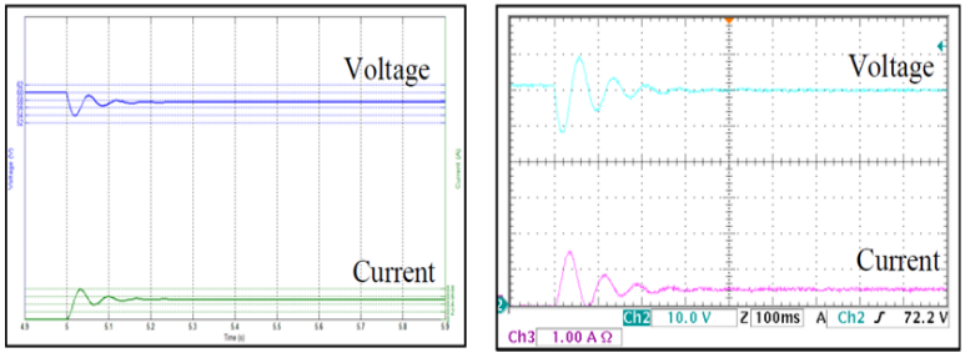
(a) (b)

Figure 7. Plot of bus voltage and current with CPL= 90 W with CPL connection without passive damper; (a) simulation (b) experiment



(a) (b)

Figure 8. Plot of bus voltage and current with CPL= 60 W with CPL connection without passive damper; (a) simulation (b) experiment



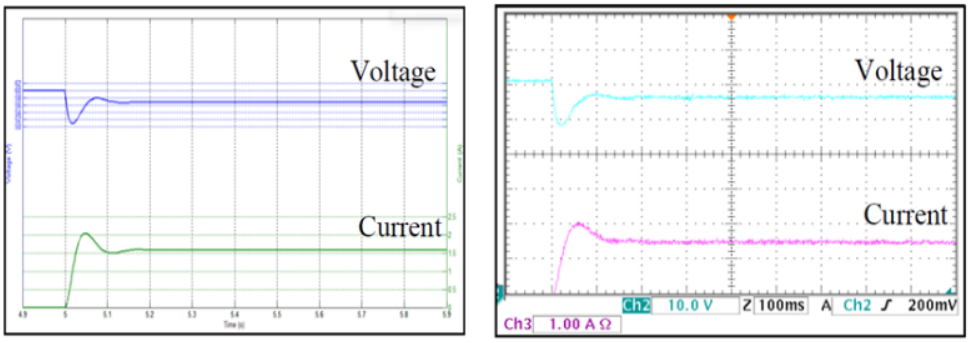
(a) (b)

Figure 9. Plot of bus voltage and current with CPL= 30 W with CPL connection without passive damper; (a) simulation (b) experiment

Table 1. Comparison between simulation and experiment in overshoot percentage, settling time and steady state error during CPL transience without passive damper

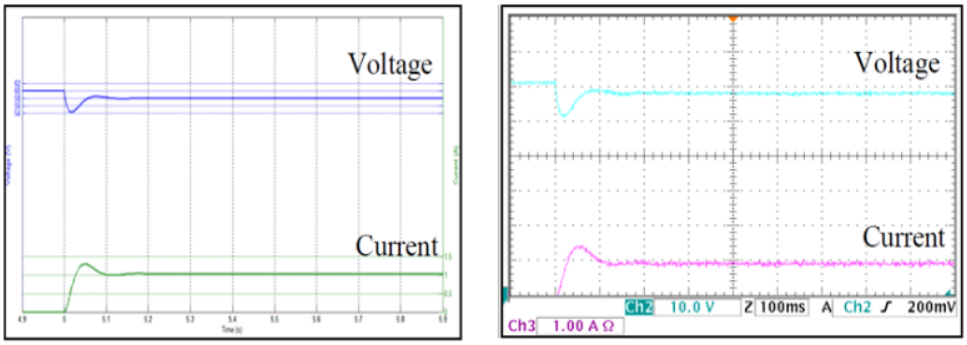
CPL Power (Watt)		90	60	30
Overshoot (%)	Simulation	28.00	9.09	3.44
	Experiment	16.07	20.68	13.33
Settling Time (s)	Simulation	0.80	0.50	0.30
	Experiment	0.60	0.60	0.40
Steady state error (%)	Simulation	16.67	8.33	3.33
	Experiment	6.67	3.33	1.67

The waveforms of simulation and experiment in Figure 10, Figure 11 and Figure 12 show the effectiveness of passive damping network in reducing the bus oscillation and makes the system more stable. Three power levels of constant power load are applied, which are 90 W, 60 W and 30 W with an input voltage supply fixed at 60 V. The comparison of DC bus voltage waveform with respect to Figure 7, Figure 8 and Figure 9 shown that the system is much more stable and the oscillation has been eliminated succesfully. The simulation results shows less overshoot when compared to the experimental results. However, there is steady state error which the bus voltages are tremendously dropped from the actual value of steady state if the CPL level is increased. This is due to noise produced by the bottom track of PCB copper board or the jumper wires used in the experiment. Table 2 presents the analysis on comparison between simulation and experiment inovershoot, settling time and steady state error with presence of passive damper.



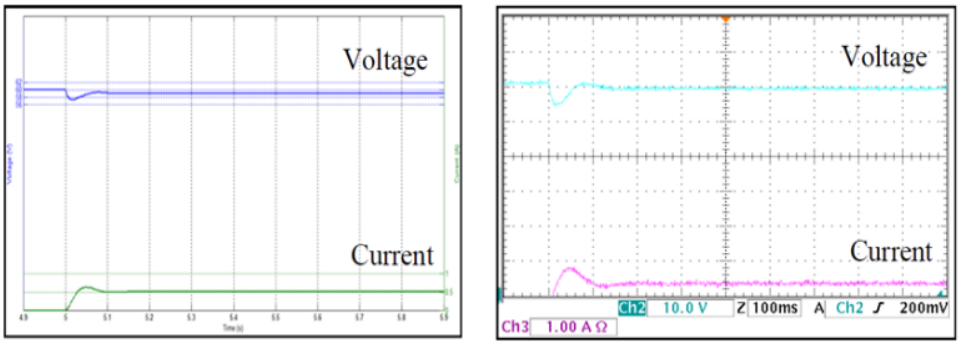
(a) (b)

Figure 10. Plot of bus voltage and current with CPL= 90 W with CPL connection with passive damper; (a) simulation (b) experiment



(a) (b)

Figure 11. Plot of bus voltage and current with CPL= 60 W with CPL connection with passive damper; (a) simulation (b) experiment



(a) (b)

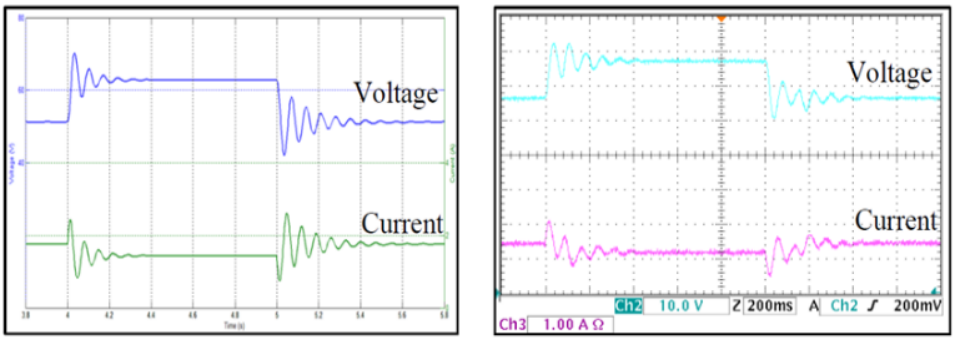
Figure 12. Plot of bus voltage and current with CPL= 30 W with CPL connection with passive damper; (a) simulation (b) experiment

Table 2. Comparison between simulation and experiment in overshoot percentage, settling time and steady state error during CPL transience with passive damper

CPL Power (Watt)		90	60	30
Overshoot (%)	Simulation	1.75	1.72	0.80
	Experiment	3.57	1.72	1.69
Settling Time (s)	Simulation	0.20	0.15	0.10
	Experiment	0.25	0.20	0.20
Steady state error (%)	Simulation	5.00	3.33	1.67
	Experiment	6.67	3.33	1.69

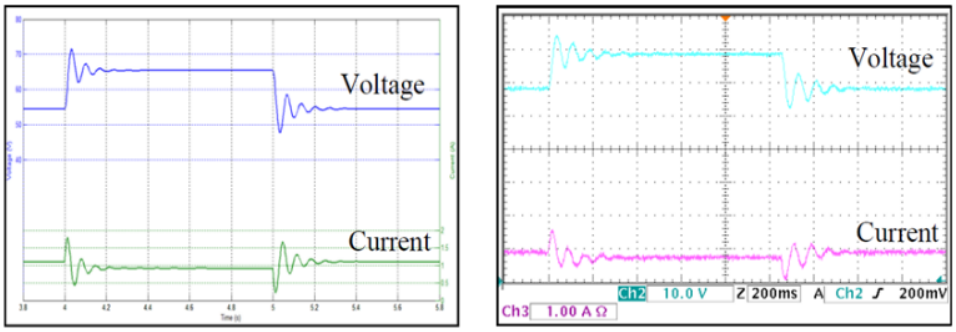
4.2. DC Bus Voltages during Positive and Negative Input Voltage Changes without and with Passive Damper and Fixed CPL Level

DC input voltage of ±10 V was used as step up and down to represent positive and negative input voltage changes respectively. The waveforms of simulation and experiment of the bus voltages and current without the connection of passive damper can be seen in Figure 13, Figure 14 and Figure 15. It experiences oscillation and ringing for positive transience and settled at 70 V while for negative transience the bus voltage drops and oscillates before it settled at 60 V with CPL power level of 90 W, 60 W and 30 W. The analysis for the changes in voltage and current for both positive and negative steps was summarized in Table 3 and Table 4.



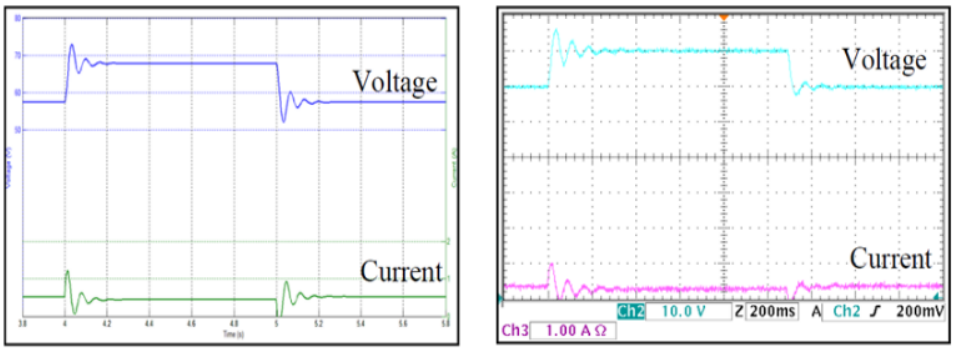
(a) (b)

Figure 13. Plot of bus voltage and current with CPL= 90 W during input voltage transience without passive damper; (a) simulation (b) experiment



(a) (b)

Figure 14. Plot of bus voltage and current with CPL= 60 W during input voltage transience without passive damper; (a) simulation (b) experiment



(a) (b)

Figure 15. Plot of bus voltage and current with CPL= 30 W during input voltage transience without passive damper; (a) simulation (b) experiment

Table 3. Comparison of CPL power level between simulation and experiment in overshoot percentage, settling time and steady state error for voltage step up without passive damper

CPL Power (Watt)		90	60	30
Overshoot (%)	Simulation	12.50	10.76	7.35
	Experiment	9.09	8.82	8.57
Settling Time (s)	Simulation	0.40	0.30	0.30
	Experiment	0.50	0.40	0.40
Steady state error (%)	Simulation	8.57	7.14	2.85
	Experiment	5.72	1.47	0.00

Table 4. Comparison of CPL power level between simulation and experiment in overshoot percentage, settling time and steady state error for voltage step down without passive damper

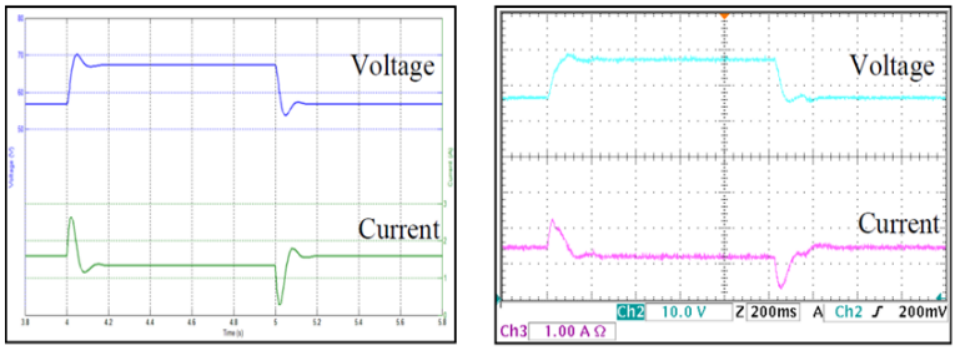
Power (Watt)		90	60	30
Overshoot (%)	Simulation	14.00	12.72	8.62
	Experiment	7.14	10.34	3.33
Settling Time (s)	Simulation	0.80	0.40	0.30
	Experiment	0.50	0.40	0.40
Steady state error (%)	Simulation	16.67	8.33	3.33
	Experiment	6.67	3.33	0.00

In the positive voltage transience, the bus voltage and current has overshoot to a maximum value and then oscillate before they gradually reduce to steady state value. However, the bus voltage and current in the

negative transience drop and then oscillate before they go to steady state value due to the inductive kick when current decrease. Other than that, there are more steady state error or bus voltage drop when higher value of CPL level is applied to both transience. The waveform satisfy the experimental results since the oscillation increases as the CPL level increases but the difference between the experimental results and simulation results is the time taken for the system to become stable and reach steady state.

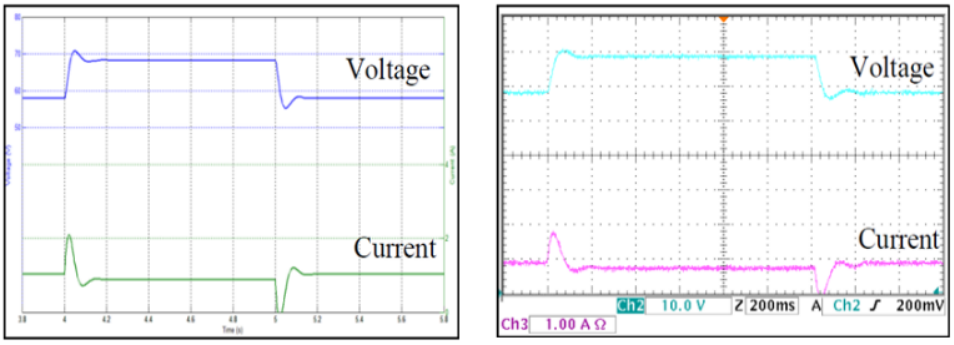
Based on previous research, when the CPL level is higher, the level of bus oscillation increased, thus the time taken for the system to reach steady state will be longer. It is clearly shown that the constant power load causes an oscillation in the system because of its negative incremental input impedance characteristic. The waveform proved that the system was not stable and it required a compensator in order to remove the oscillation generated in the system.

Figure 16, Figure 17 and Figure 18 shows that the waveform of simulation and experiments became more stable when the passive damper network is connected to the system. These waveforms shows the DC bus voltages behavior for three CPL power levels of 90 W, 60 W and 30 W respectively. Table 5 and Table 6 presents the responses comparison in simulation and experiment for positive and negative transience respectively.



(a) (b)

Figure 16. Plot of bus voltage and current with CPL= 90 W during input voltage transience with passive damper; (a) simulation (b) experiment



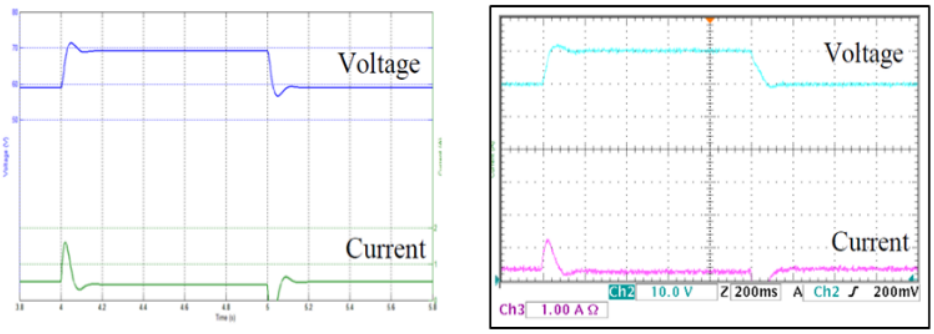
(a) (b)

Figure 17. Plot of bus voltage and current with CPL= 60 W during input voltage transience with passive damper; (a) simulation (b) experiment

Both positive and negative voltage transience of ±10 V indicated that the bus voltage have small overshoot and the system reached steady state with a less time when compared in Figure 13, Figure 14 and Figure 15, which shows the same response without passive damper network connected. However, by increasing the CPL level value, the system has small overshoot and it took longer time to reach steady state compared to

small CPL level value which almost completely eliminates the overshoot. Other than that, when value of CPL level is higher, there are more steady state error or bus voltage drop for both transience.

The waveforms satisfy the experimental results since that the overshoot increases as the power level increases but the difference between the experimental results and simulation results is only on the time taken for the system become stable to steady state. From the simulation and experiment result, it is show there is small overshoot in the bus voltage but the system is still stable for all three cases of power levels.



(a) (b)

Figure 18. Plot of bus voltage and current with CPL= 30 W during input voltage transience with passive damper; (a) simulation (b) experiment

Table 5. Comparison of CPL power level between simulation and experiment in overshoot percentage, settling time and steady state error for voltage step up with passive damper

Power (Watt)		90	60	30
Overshoot (%)	Simulation	4.47	5.88	5.79
	Experiment	3.03	2.94	2.85
Settling Time (s)	Simulation	0.30	0.20	0.20
	Experiment	0.22	0.20	0.19
Steady state error (%)	Simulation	4.28	2.85	1.42
	Experiment	5.71	2.85	0.00

Table 6. Comparison of CPL power level between simulation and experiment in overshoot percentage, settling time and steady state error for voltage step down with passive damper

Power (Watt)		90	60	30
Overshoot (%)	Simulation	1.78	3.57	1.72
	Experiment	3.57	3.03	1.67
Settling Time (s)	Simulation	0.20	0.18	0.20
	Experiment	0.24	0.24	0.18
Steady state error (%)	Simulation	6.67	6.67	3.33
	Experiment	6.67	6.67	0.00

5. CONCLUSION

The passive damping network was proposed in this paper in order to eliminate the oscillation or ringing in the DC bus voltage waveform and to improve the stability of such system. The oscillation occur in the bus waveform indicates the instability phenomena in the system due to the characteristic of CPL. The insertion of passive damping network proved that the instability occur in the system due to CPL were successfully corrected in both cases of input supply and the CPL power level changes. Initially the passive RC damper was modeled and designed. Then the performance of passive damping network was analyzed and simulated using MATLAB/Simulink. An experiment was conducted to examine the passive damper performances and the obtained results were compared with simulation results. Finally, the analysis and discussion for the system was conducted in detail. As a conclusion, the designed passive damper successfully eliminates the DC bus oscillation in DPS system in both theoretically and practically.

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